

C18 config 設定

Configuration Bits set in code

Address	Value	Field	Category	Setting
300001	02	OSC	Oscillator	HS
		FCMEN	Fail-Safe Clock Monitor Enable	Disabled
		IESO	Internal External Switch Over Mode	Disabled
300002	0E	PUT	Power Up Timer	Enabled
		BODEN	Brown Out Detect	Enabled in hardware, SBOREN disabled
		BODENV	Brown Out Voltage	4.2V
300003	1E	WDT	Watchdog Timer	Disabled- Controlled by SWDTEN bit
		WDTPS	Watchdog Postscaler	1:32768
300005	81	CCP2MUX	CCP2 Mux	RC1
		PBADEN	PortB A/D Enable	PORTB<4:0> configured as digital I/O on RESET
		LPT1OSC	Low Power Timer1 Osc enable	Disabled
		MCLR	Master Clear Enable	MCLR Enabled RE3 Disabled
300006	80	STVR	Stack Overflow Reset	Disabled
		LVP	Low Voltage Program	Disabled
		XINST	Extended Instruction Set Enable bit	Disabled
300008	00	CP_0	Code Protect 00800-01FFF	Enabled
		CP_1	Code Protect 02000-03FFF	Enabled
		CP_2	Code Protect 04000-05FFF	Enabled
		CP_3	Code Protect 06000-07FFF	Enabled
300009	80	CPB	Code Protect Boot	Enabled
		CPD	Data EEPROM Code Protect	Disabled
30000A	0F	WRT_0	Table Write Protect 00800-01FFF	Disabled
		WRT_1	Table Write Protect 02000-03FFF	Disabled
		WRT_2	Table Write Protect 04000-05FFF	Disabled
		WRT_3	Table Write Protect 06000-07FFF	Disabled
30000B	C0	WRIC	Config. Write Protect	Enabled
		WRIB	Table Write Protect Boot	Disabled
		WRID	Data EEPROM Write Protect	Disabled
30000C	0F	EBTR_0	Table Read Protect 00800-01FFF	Disabled
		EBTR_1	Table Read Protect 02000-03FFF	Disabled
		EBTR_2	Table Read Protect 04000-05FFF	Disabled
		EBTR_3	Table Read Protect 06000-07FFF	Disabled
30000D	40	EBTRB	Table Read Protect Boot	Disabled

必須設定正確的項目

APP001 config 設定値

Configuration Bits set in code

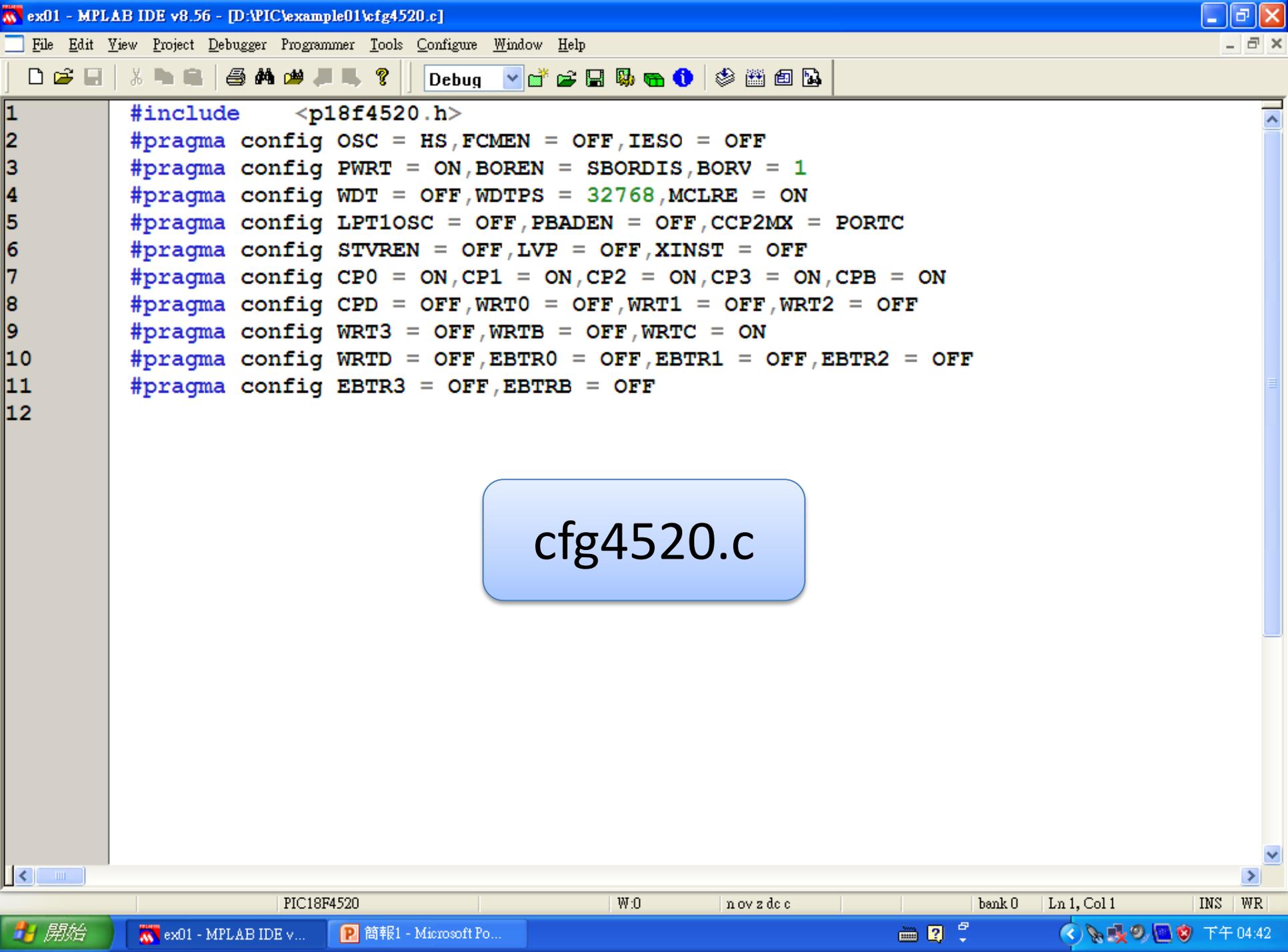
Address	Value	Field	Category	Setting
300001	02	OSC	Oscillator	HS
		FCMEN	Fail-Safe Clock Monitor Enable	Disabled
		IESO	Internal External Switch Over Mode	Disabled
300002	0E	PUT	Power Up Timer	Enabled
		BODEN	Brown Out Detect	Enabled in hardware, SBOREN disabled
		BODENV	Brown Out Voltage	4.2V
300003	1E	WDT	Watchdog Timer	Disabled-Controlled by SWDTEN bit
		WDTPS	Watchdog Postscaler	1:32768
300005	81	CCP2MUX	CCP2 Mux	RC1
		PBADEN	PortB A/D Enable	PORTB<4:0> configured as digital I/O on RESET
		LPT1OSC	Low Power Timer1 Osc enable	Disabled
		MCLRE	Master Clear Enable	MCLR Enabled, RE3 Disabled
300006	80	STVR	Stack Overflow Reset	Disabled
		LVP	Low Voltage Program	Disabled
		XINST	Extended Instruction Set Enable bit	Disabled
300008	00	CP_0	Code Protect 00800-01FFF	Enabled
		CP_1	Code Protect 02000-03FFF	Enabled
		CP_2	Code Protect 04000-05FFF	Enabled
		CP_3	Code Protect 06000-07FFF	Enabled
300009	80	CPB	Code Protect Boot	Enabled
		CPD	Data EEPROM Code Protect	Disabled
30000A	0F	WRT_0	Table Write Protect 00800-01FFF	Disabled
		WRT_1	Table Write Protect 02000-03FFF	Disabled
		WRT_2	Table Write Protect 04000-05FFF	Disabled
		WRT_3	Table Write Protect 06000-07FFF	Disabled
30000B	C0	WRIC	Config. Write Protect	Enabled
		WRIB	Table Write Protect Boot	Disabled
		WRID	Data EEPROM Write Protect	Disabled
30000C	0F	EBTR_0	Table Read Protect 00800-01FFF	Disabled
		EBTR_1	Table Read Protect 02000-03FFF	Disabled
		EBTR_2	Table Read Protect 04000-05FFF	Disabled
		EBTR_3	Table Read Protect 06000-07FFF	Disabled
30000D	40	EBTRB	Table Read Protect Boot	Disabled

PIC18F4520

W:0

nov 2 dc

bank 0



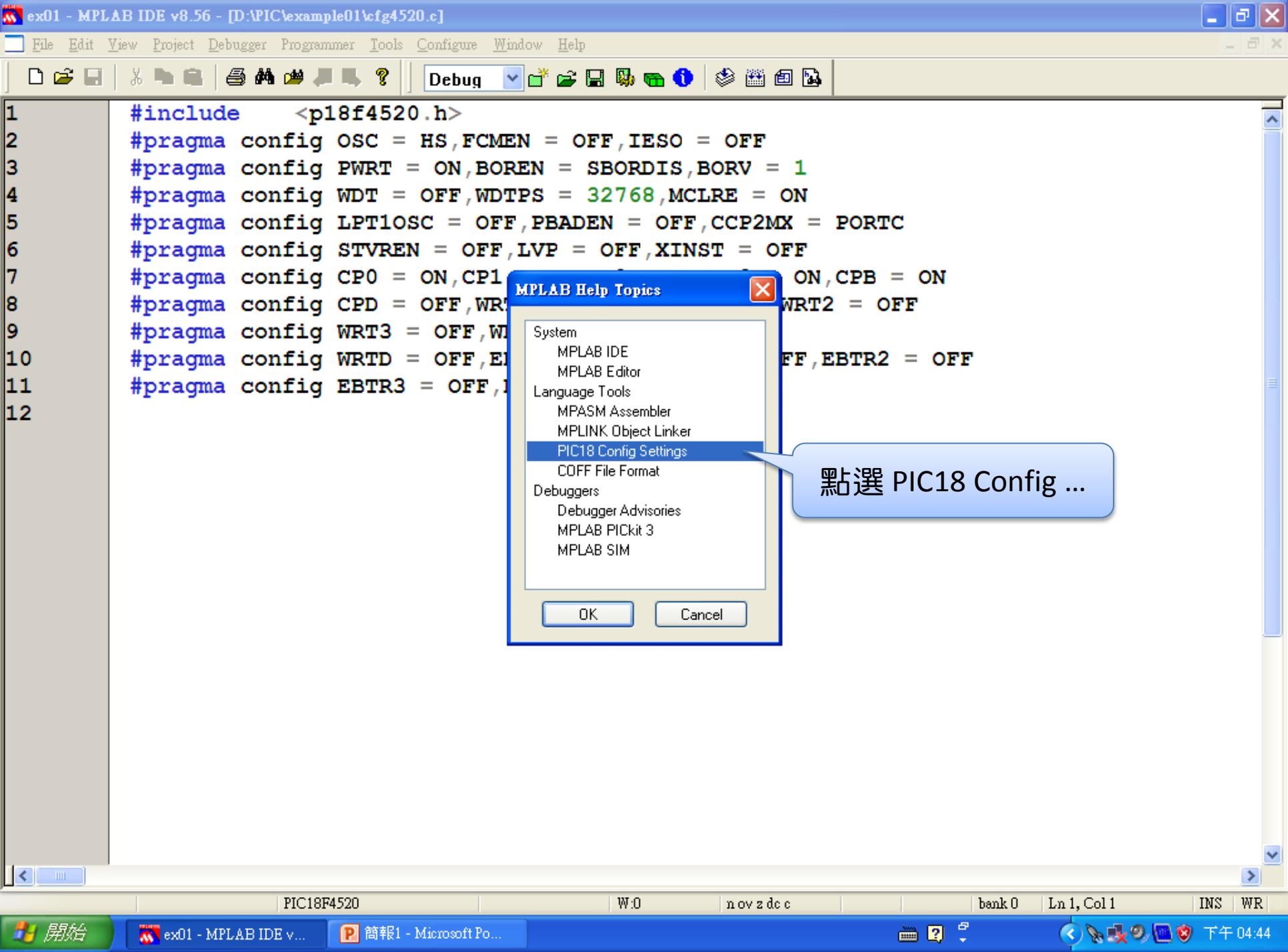
cfg4520.c

點選 Topic

```

1  #include <p18f4520.h>
2  #pragma config OSC = HS,FCMEN = OFF
3  #pragma config PWRT = ON,BOREN = OFF
4  #pragma config WDT = OFF,WDTPS = 1
5  #pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
6  #pragma config STVREN = OFF,LVP = OFF,XINST = OFF
7  #pragma config CP0 = ON,CP1 = ON,CP2 = ON,CP3 = ON,CPB = ON
8  #pragma config CPD = OFF,WRT0 = OFF,WRT1 = OFF,WRT2 = OFF
9  #pragma config WRT3 = OFF,WRTB = OFF,WRTC = ON
10 #pragma config WRTD = OFF,EBTR0 = OFF,EBTR1 = OFF,EBTR2 = OFF
11 #pragma config EBTR3 = OFF,EBTRB = OFF
12

```



MPLAB Help Topics

- System
 - MPLAB IDE
 - MPLAB Editor
- Language Tools
 - MPASM Assembler
 - MPLINK Object Linker
 - PIC18 Config Settings**
 - COFF File Format
- Debuggers
 - Debugger Advisories
 - MPLAB PICKit 3
 - MPLAB SIM

OK Cancel

點選 PIC18 Config ...

PIC18F4520

W:0

n o v a d c c

bank 0

Ln 1, Col 1

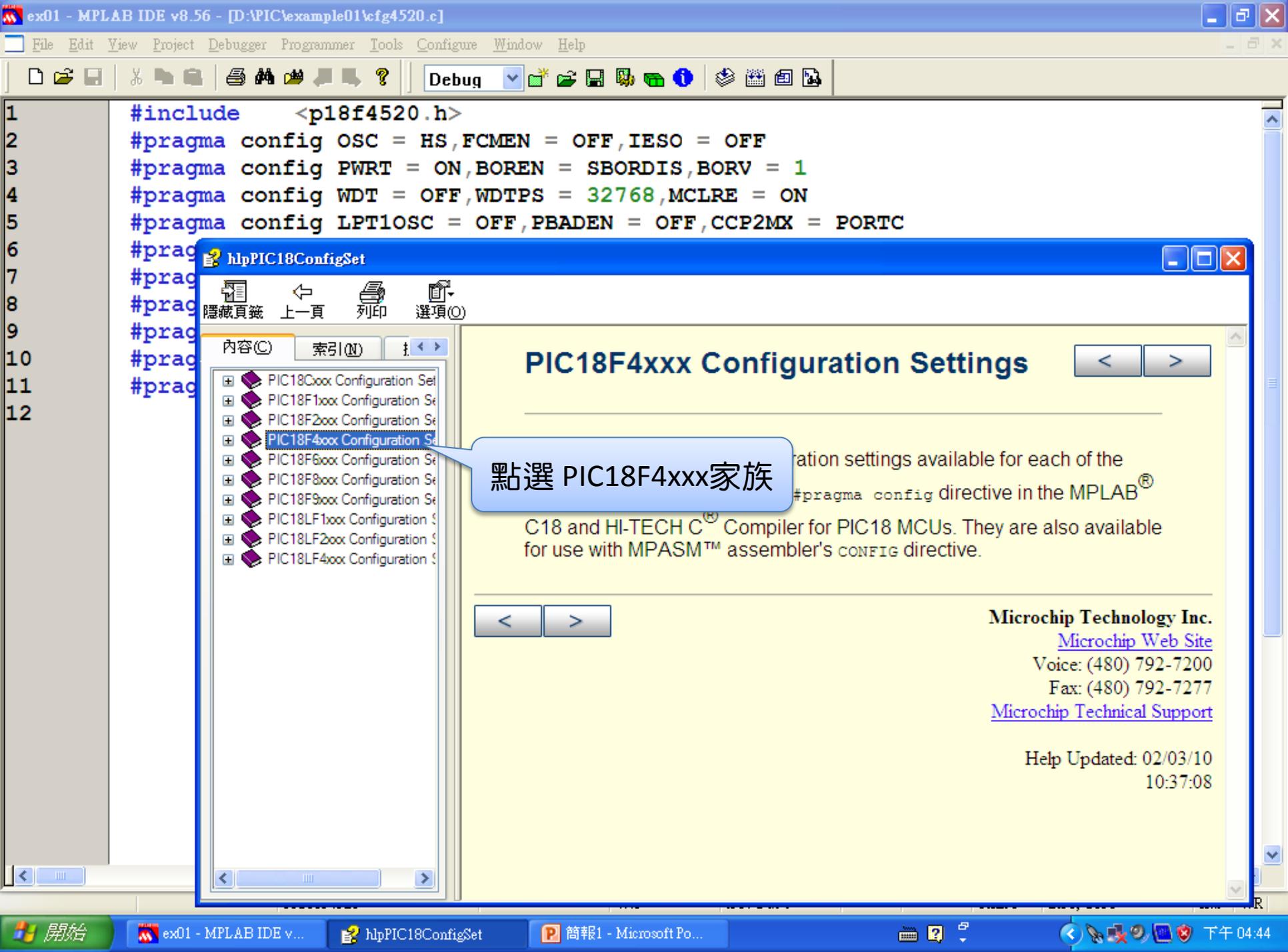
INS WR

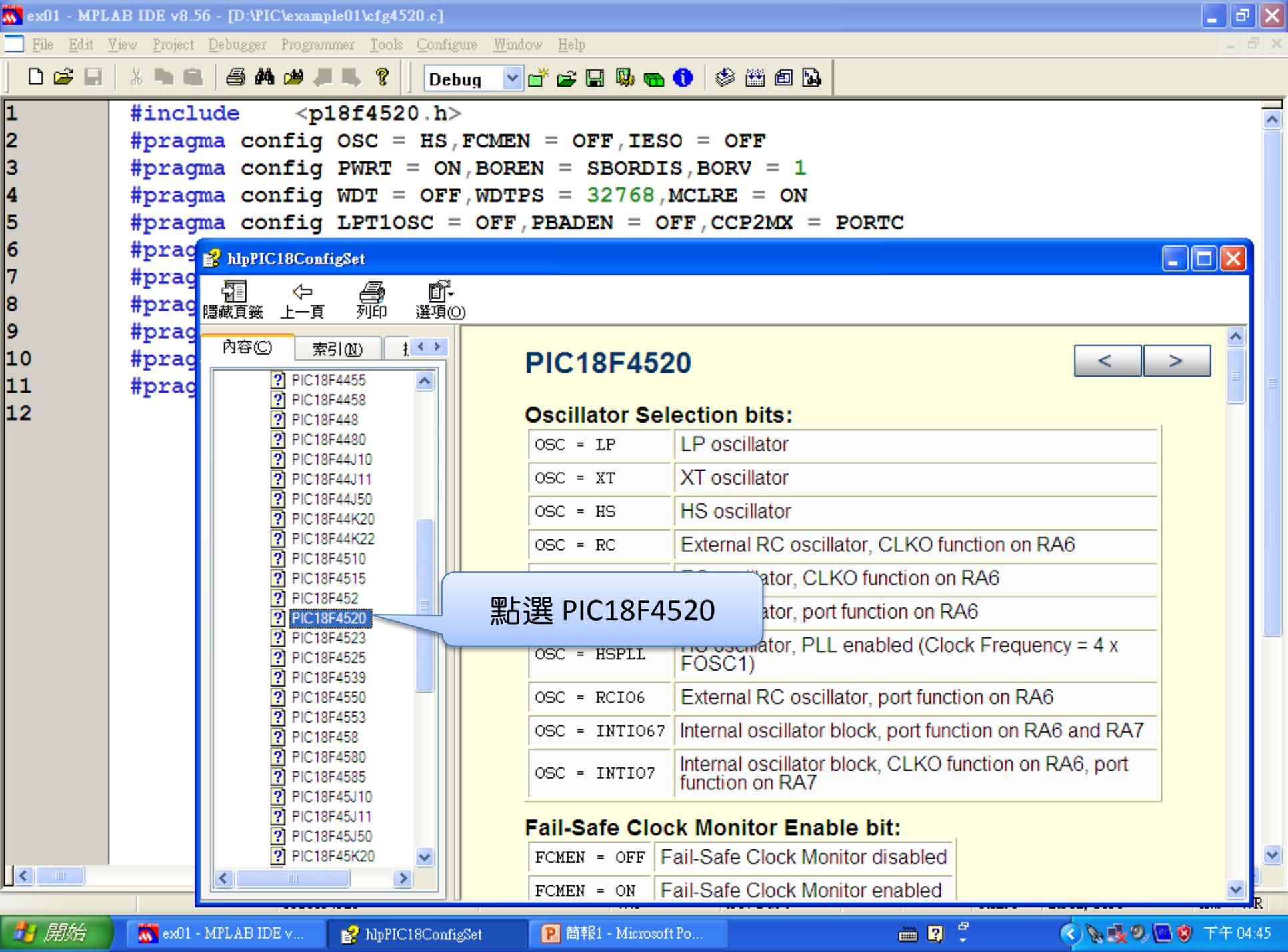
開始

ex01 - MPLAB IDE v...

簡報1 - Microsoft Po...

下午 04:44





```
1 #include <pic18f4520.h>
2 #pragma config OSC = HS,FCMEN = OFF,IESO = OFF
3 #pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
4 #pragma config WDT = OFF,WDTPS = 32768,MCLRE = ON
5 #pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
6 #pragma
7 #pragma
8 #pragma
9 #pragma
10 #pragma
11 #pragma
12
```

hlpPIC18ConfigSet

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內容(C) 索引(I)

- PIC18F4455
- PIC18F4458
- PIC18F448
- PIC18F4480
- PIC18F44J10
- PIC18F44J11
- PIC18F44J50
- PIC18F44K20
- PIC18F44K22
- PIC18F4510
- PIC18F4515
- PIC18F452
- PIC18F4520**
- PIC18F4523
- PIC18F4525
- PIC18F4539
- PIC18F4550
- PIC18F4553
- PIC18F458
- PIC18F4580
- PIC18F4585
- PIC18F45J10
- PIC18F45J11
- PIC18F45J50
- PIC18F45K20

PIC18F4520

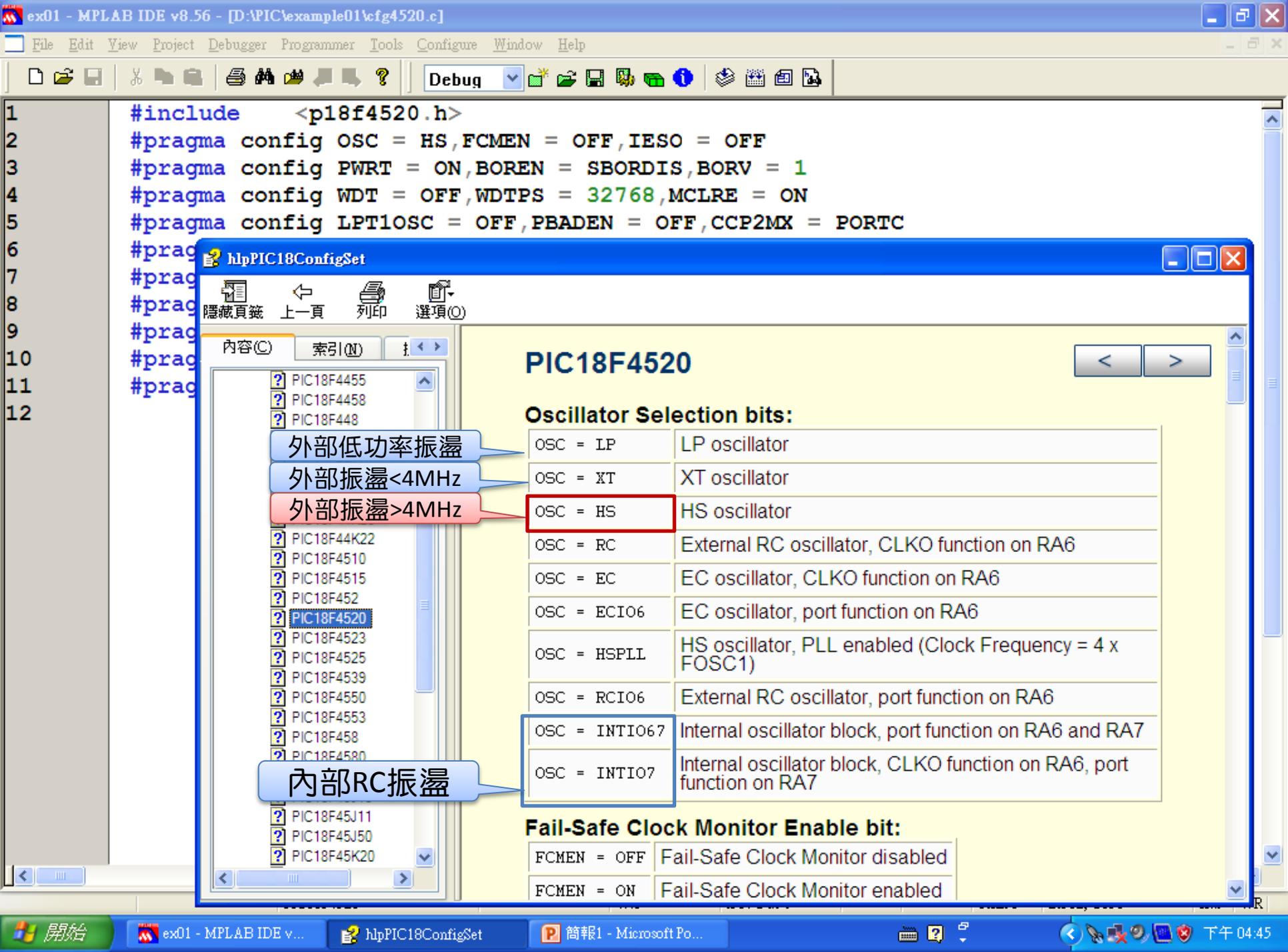
Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = RCIO6	External RC oscillator, port function on RA6
OSC = INTIO67	Internal oscillator block, port function on RA6 and RA7
OSC = INTIO7	Internal oscillator block, CLKO function on RA6, port function on RA7
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

點選 PIC18F4520



```
1 #include <p18f4520.h>
2 #pragma config OSC = HS,FCMEN = OFF,IESO = OFF
3 #pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
4 #pragma config WDT = OFF,WDTPS = 32768,MCLRE = ON
5 #pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
6 #pragma
7 #pragma
8 #pragma
9 #pragma
10 #pragma
11 #pragma
12
```

PIC18F4520

Oscillator Selection bits:

OSC = LP	LP oscillator
OSC = XT	XT oscillator
OSC = HS	HS oscillator
OSC = RC	External RC oscillator, CLKO function on RA6
OSC = EC	EC oscillator, CLKO function on RA6
OSC = ECI06	EC oscillator, port function on RA6
OSC = HSPLL	HS oscillator, PLL enabled (Clock Frequency = 4 x FOSC1)
OSC = RCI06	External RC oscillator, port function on RA6
OSC = INTI067	Internal oscillator block, port function on RA6 and RA7
OSC = INTI07	Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF	Fail-Safe Clock Monitor disabled
FCMEN = ON	Fail-Safe Clock Monitor enabled

外部低功率振盪

外部振盪 < 4MHz

外部振盪 > 4MHz

內部RC振盪

Configuration Bits set in code.

Address	Value	Field	Category	Setting
300001	02	OSC	Oscillator	HS
		FCMEN	Fail-Safe Clock Monitor Enable	Disabled
		IESO	Internal External Switch Over Mode	Disabled
300002	0E	PUT	Power Up Timer	Enabled

hlpPIC18ConfigSet

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內容(C) 索引(I) 目錄(D)

- [PIC18F4455](#)
- [PIC18F4458](#)
- [PIC18F448](#)
- [PIC18F4480](#)
- [PIC18F44J10](#)
- [PIC18F44J11](#)
- [PIC18F44J50](#)
- [PIC18F44K20](#)
- [PIC18F44K22](#)
- [PIC18F4510](#)
- [PIC18F4515](#)
- [PIC18F452](#)
- [PIC18F4520](#)
- [PIC18F4523](#)
- [PIC18F4525](#)
- [PIC18F4539](#)
- [PIC18F4550](#)
- [PIC18F4553](#)
- [PIC18F458](#)
- [PIC18F4580](#)
- [PIC18F4585](#)
- [PIC18F45J10](#)
- [PIC18F45J11](#)
- [PIC18F45J50](#)
- [PIC18F45K20](#)

OSC = INTIO7 Internal oscillator block, CLKO function on RA6, port function on RA7

Fail-Safe Clock Monitor Enable bit:

FCMEN = OFF Fail-Safe Clock Monitor disabled

FCMEN = ON Fail-Safe Clock Monitor enabled

Internal/External Oscillator Switchover bit:

IESO = OFF Oscillator Switchover mode disabled

IESO = ON Oscillator Switchover mode enabled

Power-up Timer Enable bit:

PWRT = ON PWRT enabled

PWRT = OFF PWRT disabled

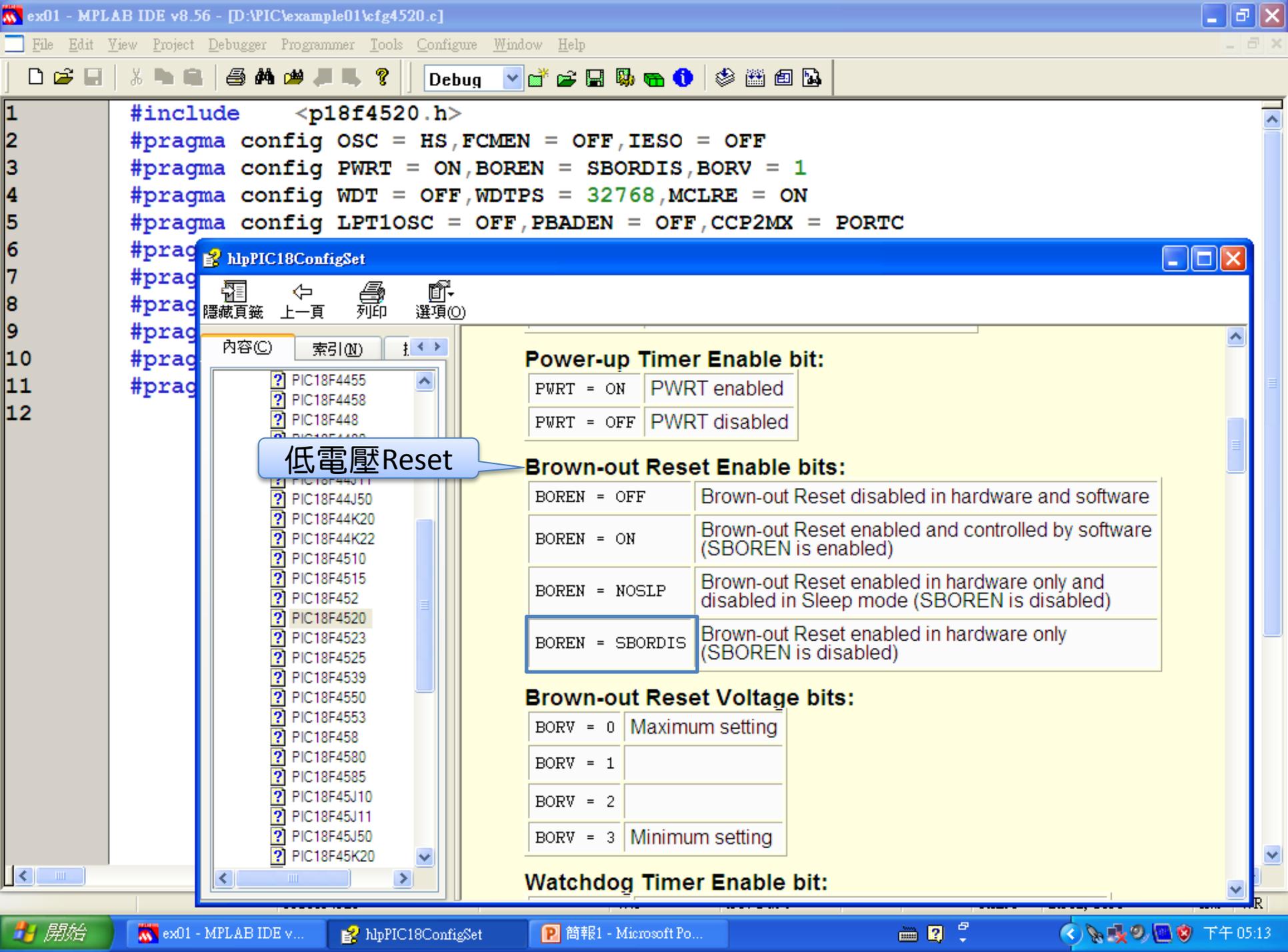
Brown-out Reset Enable bits:

BOREN = OFF Brown-out Reset disabled in hardware and software

BOREN = ON Brown-out Reset enabled and controlled by software (SBOREN is enabled)

BOREN = NOSLP Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)

BOREN = SBOREN Brown-out Reset enabled in hardware only



```
1 #include <p18f4520.h>
2 #pragma config OSC = HS,FCMEN = OFF,IESO = OFF
3 #pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
4 #pragma config WDT = OFF,WDTPS = 32768,MCLRE = ON
5 #pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
6 #pragma
7 #pragma
8 #pragma
9 #pragma
10 #pragma
11 #pragma
12
```

hlpPIC18ConfigSet

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內容(C) 索引(I)

- PIC18F4455
- PIC18F4458
- PIC18F448
- PIC18F4482
- PIC18F4520**
- PIC18F4523
- PIC18F4525
- PIC18F4539
- PIC18F4550
- PIC18F4553
- PIC18F458
- PIC18F4580
- PIC18F4585
- PIC18F45J10
- PIC18F45J11
- PIC18F45J50
- PIC18F45K20

Power-up Timer Enable bit:

PWRT = ON	PWRT enabled
PWRT = OFF	PWRT disabled

Brown-out Reset Enable bits:

BOREN = OFF	Brown-out Reset disabled in hardware and software
BOREN = ON	Brown-out Reset enabled and controlled by software (SBOREN is enabled)
BOREN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
BOREN = SBORDIS	Brown-out Reset enabled in hardware only (SBOREN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting
BORV = 1	
BORV = 2	
BORV = 3	Minimum setting

Watchdog Timer Enable bit:

低電壓Reset

ex01 - MPLAB IDE v8.56 - [Configuration Bits]

File Edit View Project Debugger Programmer Tools Configure Window Help

Debug

1 #include <configuration.h>
 2 #pragma config
 3 #pragma config
 4 #pragma config
 5 #pragma config
 6 #pragma config
 7 #pragma config
 8 #pragma config
 9 #pragma config
 10 #pragma config
 11 #pragma config
 12

Field	Category	Setting
OSC	Oscillator	HS
FCMEN	Fail-Safe Clock Monitor Enable	Disabled
IESO	Internal External Switch Over Mode	Disabled
PUT	Power Up Timer	Enabled
BODEN	Brown Out Detect	Enabled in hardware, SBODEN disabled
BODENV	Brown Out Voltage	4.2V
WDT	Watchdog Timer	2.0V
WDTPS	Watchdog Postscaler	2.7V
CCP2MUX	CCP2 Mux	4.2V
PBADEN	PortB A/D Enable	4.5V
LPT1OSC	Low Power Timer1 Osc enable	Disabled
MCLRRE	Master Clear Enable	MCLR Enabled, RE3 Disabled

PWRT = OFF	PWRT disabled
------------	---------------

Brown-out Reset Enable bits:

BODEN = OFF	Brown-out Reset disabled in hardware and software
BODEN = ON	Brown-out Reset enabled and controlled by software (SBODEN is enabled)
BODEN = NOSLP	Brown-out Reset enabled in hardware only and disabled in Sleep mode (SBODEN is disabled)
BODEN = SBODIS	Brown-out Reset enabled in hardware only (SBODEN is disabled)

Brown-out Reset Voltage bits:

BORV = 0	Maximum setting	4.5V
BORV = 1		4.2V
BORV = 2		2.7V
BORV = 3	Minimum setting	2.0V

低電壓 Reset電壓設定值

```

1 #include <p18f4520.h>
2 #pragma config OSC = HS,FCMEN = OFF,IESO = OFF
3 #pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
4 #pragma config WDT = OFF,WDTPS = 32768,MCLRE = ON
5 #pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
6 #pragma
7 #pragma
8 #pragma
9 #pragma
10 #pragma
11 #pragma
12 #pragma

```

hlpPIC18ConfigSet

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內容(C) 索引(I)

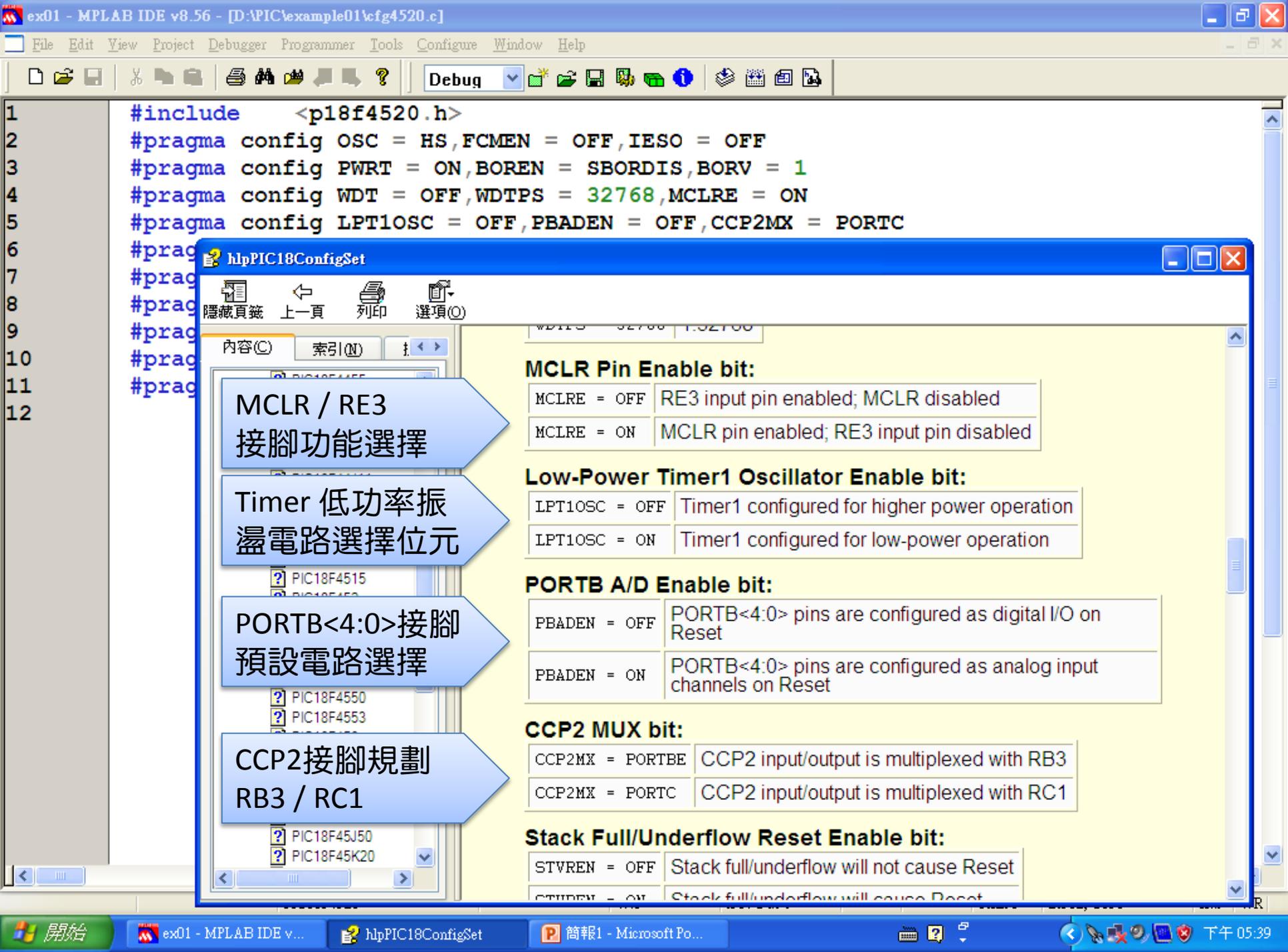
- PIC18F4455
- PIC18F4458
- PIC18F448
- PIC18F4480
- PIC18F44J10
- PIC18F44J11
- PIC18F44J50
- PIC18F44K20
- PIC18F44K22
- PIC18F4510
- PIC18F4515
- PIC18F452
- PIC18F4520
- PIC18F4523
- PIC18F4525
- PIC18F4539
- PIC18F4550
- PIC18F4553
- PIC18F458
- PIC18F4580
- PIC18F4585
- PIC18F45J10
- PIC18F45J11
- PIC18F45J50
- PIC18F45K20

Watchdog Timer Enable bit: 看門狗計時器 Reset 功能

WDT = OFF	WDT disabled (control is placed on the SWDTEN bit)
WDT = ON	WDT enabled

Watchdog Timer Postscale Select bits: 看門狗計時器，預除率選擇

WDTPS = 1	1:1
WDTPS = 2	1:2
WDTPS = 4	1:4
WDTPS = 8	1:8
WDTPS = 16	1:16
WDTPS = 32	1:32
WDTPS = 64	1:64
WDTPS = 128	1:128
WDTPS = 256	1:256
WDTPS = 512	1:512
WDTPS = 1024	1:1024
WDTPS = 2048	1:2048



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```
#include <p18f4520.h>
#pragma config OSC = HS,FCMEN = OFF,IESO = OFF
#pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
#pragma config WDT = OFF,WDTPS = 32768,MCLRE = ON
#pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
```

hlpPIC18ConfigSet

內容 索引

MCLR Pin Enable bit:

MCLRE = OFF	RE3 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RE3 input pin disabled

Low-Power Timer1 Oscillator Enable bit:

LPT1OSC = OFF	Timer1 configured for higher power operation
LPT1OSC = ON	Timer1 configured for low-power operation

PORTB A/D Enable bit:

PBADEN = OFF	PORTB<4:0> pins are configured as digital I/O on Reset
PBADEN = ON	PORTB<4:0> pins are configured as analog input channels on Reset

CCP2 MUX bit:

CCP2MX = PORTBE	CCP2 input/output is multiplexed with RB3
CCP2MX = PORTC	CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

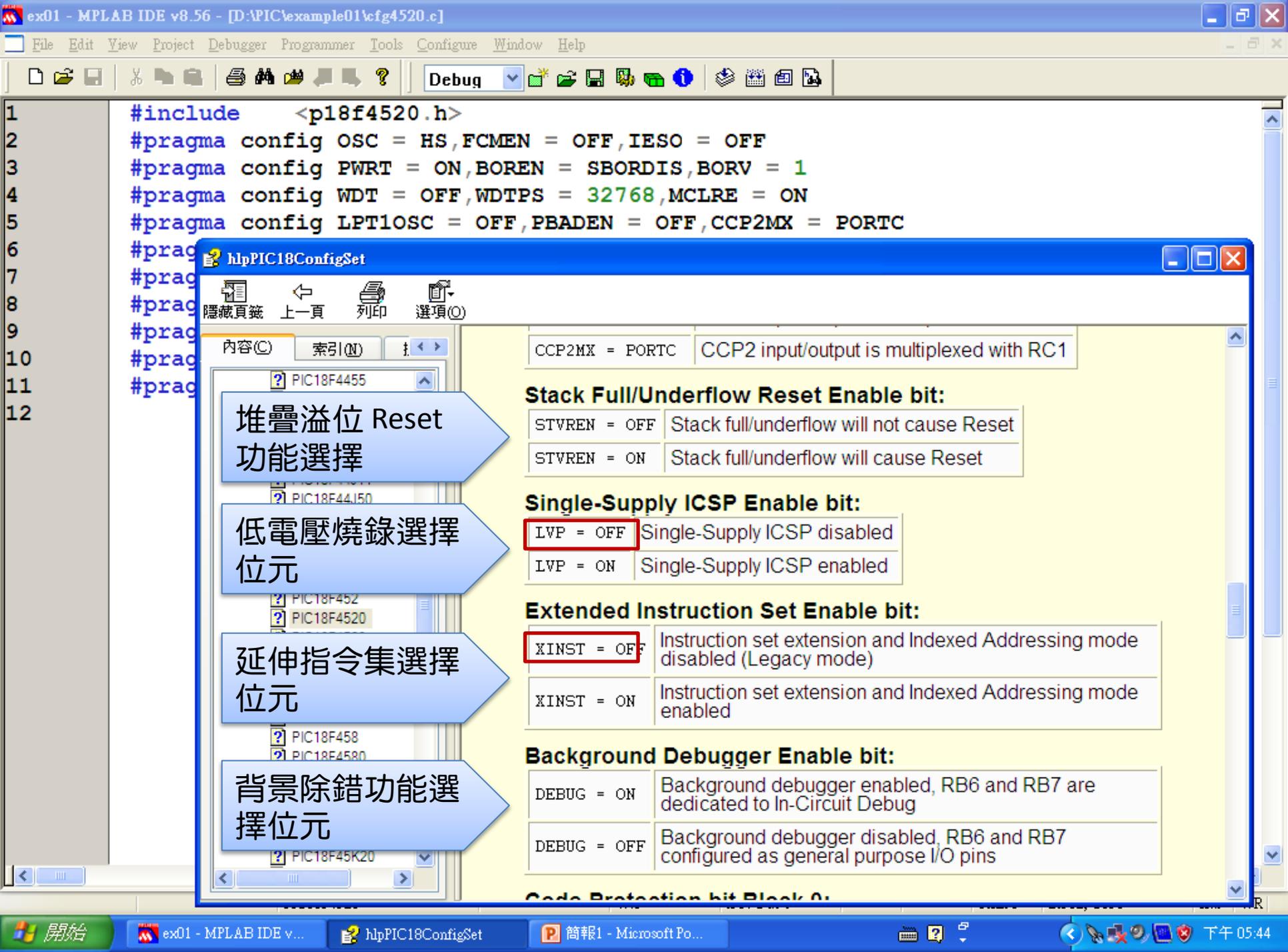
STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

MCLR / RE3
接腳功能選擇

Timer 低功率振
盪電路選擇位元

PORTB<4:0>接腳
預設電路選擇

CCP2接腳規劃
RB3 / RC1



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```
#include <p18f4520.h>
#pragma config OSC = HS,FCMEN = OFF,IESO = OFF
#pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
#pragma config WDT = OFF,WDTPS = 32768,MCLRE = ON
#pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
#pragma
#pragma
#pragma
#pragma
#pragma
```

hlpPIC18ConfigSet

內容 索引 列表

PIC18F4455

CCP2MX = PORTC CCP2 input/output is multiplexed with RC1

Stack Full/Underflow Reset Enable bit:

STVREN = OFF	Stack full/underflow will not cause Reset
STVREN = ON	Stack full/underflow will cause Reset

Single-Supply ICSP Enable bit:

LVP = OFF	Single-Supply ICSP disabled
LVP = ON	Single-Supply ICSP enabled

Extended Instruction Set Enable bit:

XINST = OFF	Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
XINST = ON	Instruction set extension and Indexed Addressing mode enabled

Background Debugger Enable bit:

DEBUG = ON	Background debugger enabled, RB6 and RB7 are dedicated to In-Circuit Debug
DEBUG = OFF	Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins

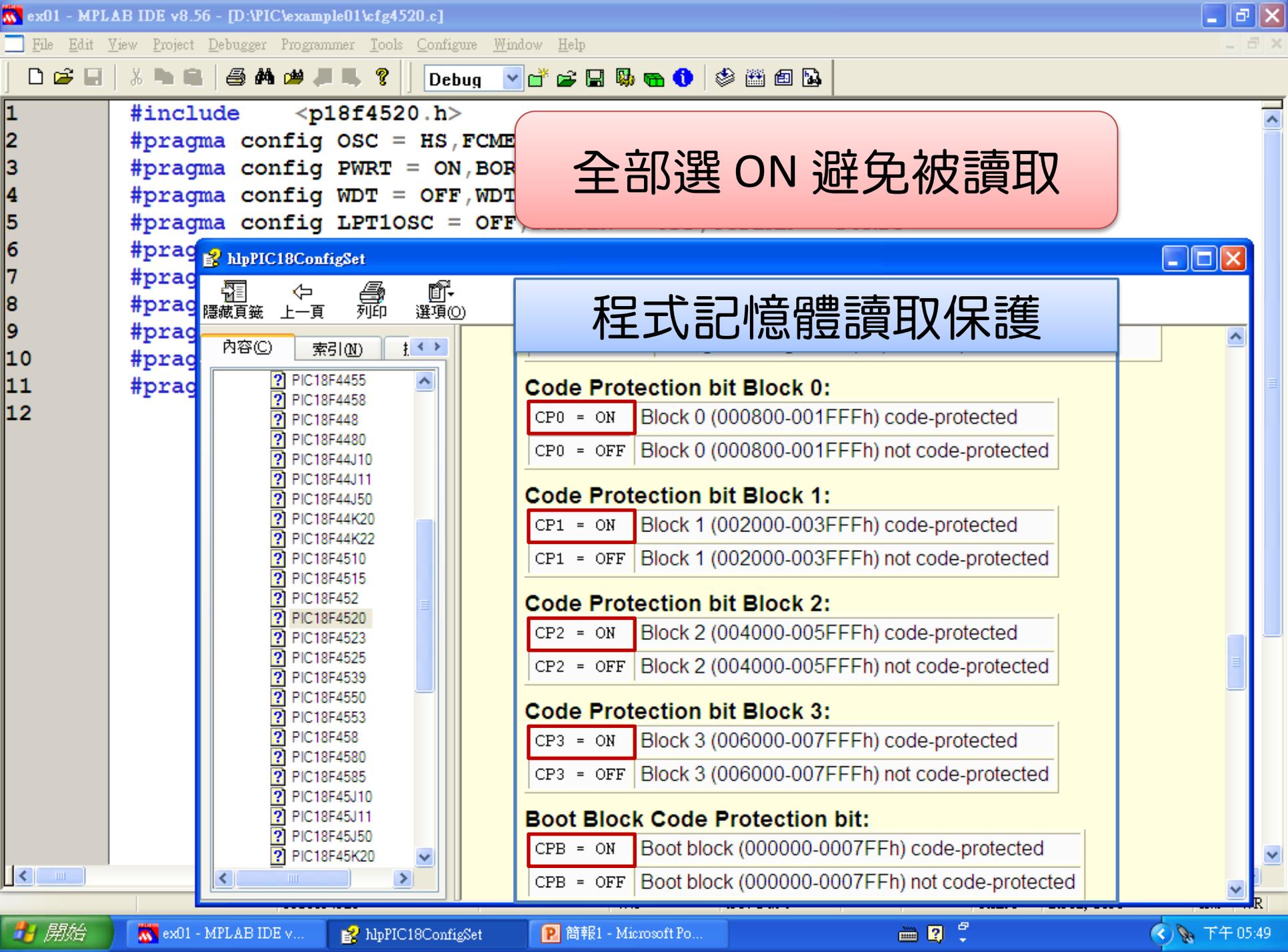
Code Protection bit Block 0:

堆疊溢位 Reset 功能選擇

低電壓燒錄選擇位元

延伸指令集選擇位元

背景除錯功能選擇位元



全部選 ON 避免被讀取

程式記憶體讀取保護

Code Protection bit Block 0:

CP0 = ON Block 0 (000800-001FFFh) code-protected
 CP0 = OFF Block 0 (000800-001FFFh) not code-protected

Code Protection bit Block 1:

CP1 = ON Block 1 (002000-003FFFh) code-protected
 CP1 = OFF Block 1 (002000-003FFFh) not code-protected

Code Protection bit Block 2:

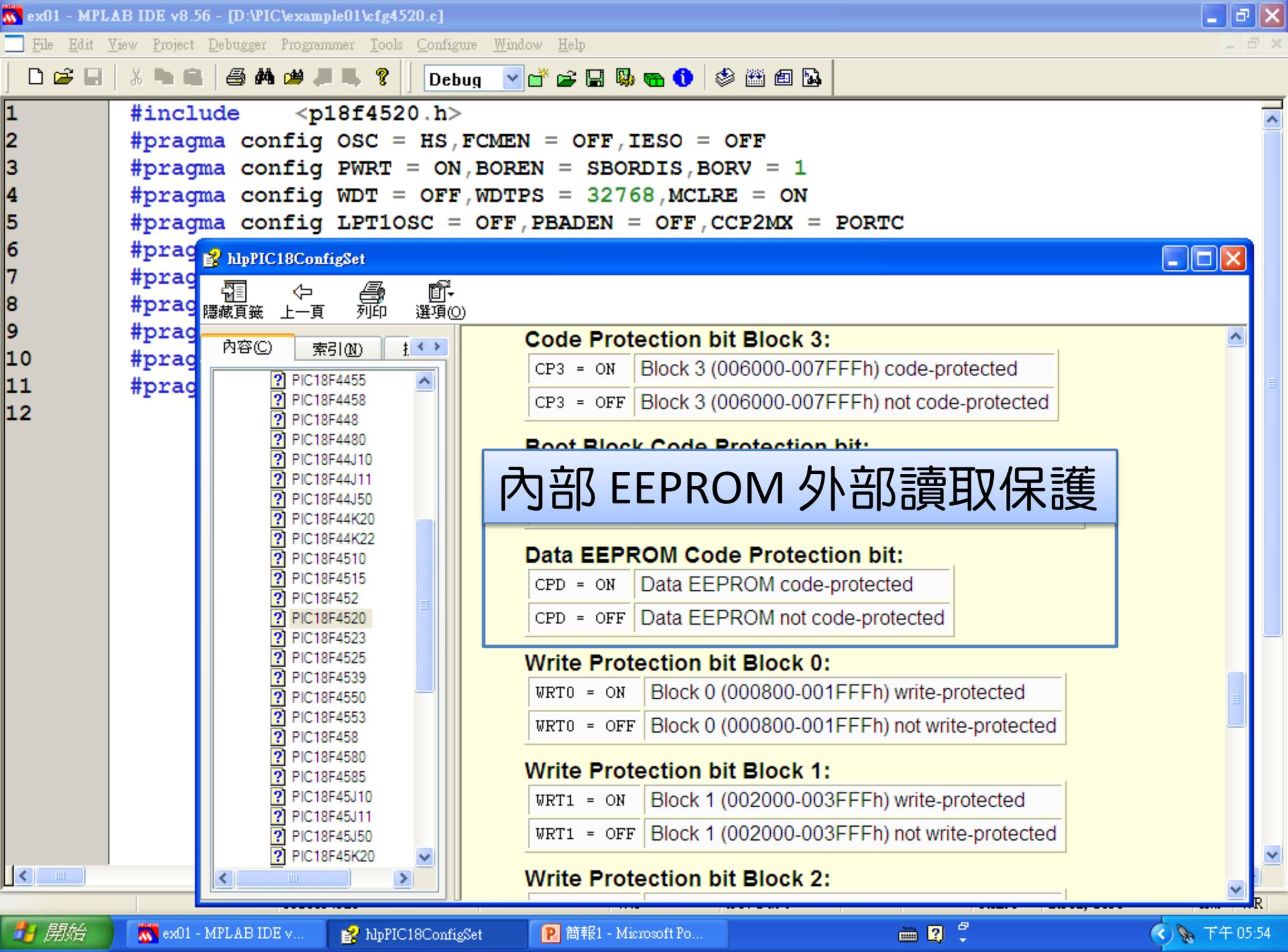
CP2 = ON Block 2 (004000-005FFFh) code-protected
 CP2 = OFF Block 2 (004000-005FFFh) not code-protected

Code Protection bit Block 3:

CP3 = ON Block 3 (006000-007FFFh) code-protected
 CP3 = OFF Block 3 (006000-007FFFh) not code-protected

Boot Block Code Protection bit:

CPB = ON Boot block (000000-0007FFFh) code-protected
 CPB = OFF Boot block (000000-0007FFFh) not code-protected



```
1 #include <p18f4520.h>
2 #pragma config OSC = HS,FCMEN = OFF,IESO = OFF
3 #pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
4 #pragma config WDT = OFF,WDTPS = 32768,MCLR = ON
5 #pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
6 #pragma
7 #pragma
8 #pragma
9 #pragma
10 #pragma
11 #pragma
12
```

hlpPIC18ConfigSet

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內容(C) 索引(I) 找 <>

- PIC18F4455
- PIC18F4458
- PIC18F448
- PIC18F4480
- PIC18F44J10
- PIC18F44J11
- PIC18F44J50
- PIC18F44K20
- PIC18F44K22
- PIC18F4510
- PIC18F4515
- PIC18F452
- PIC18F4520
- PIC18F4523
- PIC18F4525
- PIC18F4539
- PIC18F4550
- PIC18F4553
- PIC18F458
- PIC18F4580
- PIC18F4585
- PIC18F45J10
- PIC18F45J11
- PIC18F45J50
- PIC18F45K20

Code Protection bit Block 3:

CP3 = ON	Block 3 (006000-007FFFh) code-protected
CP3 = OFF	Block 3 (006000-007FFFh) not code-protected

Root Block Code Protection bit:

內部 EEPROM 外部讀取保護

Data EEPROM Code Protection bit:

CPD = ON	Data EEPROM code-protected
CPD = OFF	Data EEPROM not code-protected

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

檔案 常用 插入 設計 切換 動畫 投影片放映 校閱 檢視 開發人員 增益集

貼上 新增 剪貼簿 投影片 版面配置 重設 章節 字型 段落 繪圖 圖樣 排列 快速樣式 圖樣效果 圖樣外框 圖樣填滿 圖樣效果 尋找 取代 選取 編輯

投影片 大綱

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投影片 16/20 "Office 佈

ex01 - MPLAB IDE v8.56 - [D:\PIC\example01\cfg4520.c]

hlpPIC18ConfigSet

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內容 索引

- PIC18F4455
- PIC18F4458
- PIC18F448
- PIC18F4480
- PIC18F44J10
- PIC18F44J11
- PIC18F44J50
- PIC18F44K20
- PIC18F44K22
- PIC18F4510
- PIC18F4515
- PIC18F452
- PIC18F4520
- PIC18F4523
- PIC18F4525
- PIC18F4539
- PIC18F4550
- PIC18F4553
- PIC18F458
- PIC18F4580
- PIC18F4585
- PIC18F45J10
- PIC18F45J11
- PIC18F45J50
- PIC18F45K20

程式記憶體自我燒錄功能保護

Write Protection bit Block 0:

WRT0 = ON	Block 0 (000800-001FFFh) write-protected
WRT0 = OFF	Block 0 (000800-001FFFh) not write-protected

Write Protection bit Block 1:

WRT1 = ON	Block 1 (002000-003FFFh) write-protected
WRT1 = OFF	Block 1 (002000-003FFFh) not write-protected

Write Protection bit Block 2:

WRT2 = ON	Block 2 (004000-005FFFh) write-protected
WRT2 = OFF	Block 2 (004000-005FFFh) not write-protected

Write Protection bit Block 3:

WRT3 = ON	Block 3 (006000-007FFFh) write-protected
WRT3 = OFF	Block 3 (006000-007FFFh) not write-protected

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFh) write-protected
WRTB = OFF	Boot block (000000-0007FFh) not write-protected

Configuration Register Write Protection bit:

```

1 #include <p18f4520.h>
2 #pragma config OSC = HS,FCMEN = OFF,IESO = OFF
3 #pragma config PWRT = ON,BOREN = SBORDIS,BORV = 1
4 #pragma config WDT = OFF,WDTPS = 32768,MCLRE = ON
5 #pragma config LPT1OSC = OFF,PBADEN = OFF,CCP2MX = PORTC
6 #pragma
7 #pragma
8 #pragma
9 #pragma
10 #pragma
11 #pragma
12 #pragma

```

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- PIC18F45K20

Boot Block Write Protection bit:

WRTB = ON	Boot block (000000-0007FFh) write-protected
WRTB = OFF	Boot block (000000-0007FFh) not write-protected

Configuration Register Write Protection bit:

WRTC = ON	Configuration registers (300000-3000FFh) write-protected
WRTC = OFF	Configuration registers (300000-3000FFh) not write-protected

Data EEPROM Write Protection bit:

WRTE = ON	Data EEPROM write-protected
WRTE = OFF	Data EEPROM not write-protected

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
------------	--

```

1 #incl
2 #prag
3 #prag
4 #prag
5 #prag
6 #prag
7 #prag
8 #prag
9 #prag
10 #prag
11 #prag
12

```

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- [PIC18F4553](#)
- [PIC18F458](#)
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- [PIC18F4585](#)
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- [PIC18F45J11](#)
- [PIC18F45J50](#)
- [PIC18F45K20](#)
- [PIC18F45K22](#)
- [PIC18F45K80](#)
- [PIC18F4610](#)
- [PIC18F4620](#)
- [PIC18F4680](#)
- [PIC18F4682](#)
- [PIC18F4685](#)
- [PIC18F46J11](#)
- [PIC18F46J13](#)

Table Read Protection bit Block 0:

EBTR0 = ON	Block 0 (000800-001FFFh) protected from table reads executed in other blocks
EBTR0 = OFF	Block 0 (000800-001FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 1:

EBTR1 = ON	Block 1 (002000-003FFFh) protected from table reads executed in other blocks
EBTR1 = OFF	Block 1 (002000-003FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 2:

EBTR2 = ON	Block 2 (004000-005FFFh) protected from table reads executed in other blocks
EBTR2 = OFF	Block 2 (004000-005FFFh) not protected from table reads executed in other blocks

Table Read Protection bit Block 3:

EBTR3 = ON	Block 3 (006000-007FFFh) protected from table reads executed in other blocks
EBTR3 = OFF	Block 3 (006000-007FFFh) not protected from table reads executed in other blocks

Boot Block Table Read Protection bit:

EBTRB = ON	Boot block (000000-0007FFFh) protected from table reads executed in other blocks
EBTRB = OFF	Boot block (000000-0007FFFh) not protected from table reads executed in other blocks